# Cryogenic CMOS for scalable quantum control systems

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In this poster, we share our system level perspective on quantum control electronics, together with our most recent work on cryogenic CMOS design at IBM Zurich Research Lab. We present our progress in the design of control and readout integrated circuits for spin-based quantum computers. CMOS circuits must be designed to operate at 4 K, delivering similar performance as at industry standard process-voltage-temperature (PVT) corners. The unavailability of compact device models at cryogenic temperatures poses a major challenge on the chip design methodology. Therefore, we investigated the cryogenic characteristics of bulk-FinFETs and on-chip passive elements down to 40 mK. Our findings relevant for cryogenic CMOS circuit design will be summarized.

Spin systems have the advantage of being able to operate at higher temperatures, around 1 – 4 K. Cryogenic CMOS is a promising candidate for control and readout of spin qubits, owing to their scalability and potential to be co-packaged. Dominant problems in this scenario are thermal loading and crosstalk. Moreover, the power budget of cryogenic control electronics is limited by the available cooling power of the cryostat. Low power operation being the main motivation of cryogenic CMOS design community, novel architectures of qubit control and readout systems are being studied.

To explore qubit control, we develop radio frequency digital to analog converters (RF DAC), such as SRAM based source series terminated (SST) DAC. Such digitally assisted designs reap the scaling benefits of advanced CMOS nodes like 14 nm FinFET or below. The SST transmitter can be used to generate control pulses at 4 K. Their wide band operation from 2 GHz to 18 GHz, meet the frequency specifications of current spin qubit systems. Wide-band transmitters with sufficient spurious free dynamic range can potentially control multiple qubits through frequency division multiplexing. We discuss the benefits and challenges of this type of architecture to achieve coherent control.

Dispersive readout techniques for spin systems are preferred, owing to their synergy with super conducting systems. Frequency multiplexed readout with sufficient dynamic range offers a scalable solution. The qubit readout chain demands several amplification stages to digitize small signal levels of 10’s of microvolts to 100’s of millivolts at the ADC input. In addition to an InP HEMT LNA, we propose a cascaded inverter-based CMOS LNA stage that delivers an amplification of 58 dB. A high impedance matching consideration between the HEMT LNA and the cryogenic CMOS receiver can provide a path toward an integrated qubit readout digitizer.

The digitizer design for high fidelity readout needs careful consideration of the overall signal to noise ratio requirements of the system. Voltage controlled ring oscillator (VCRO) based ADC is one of our preferred candidates for digitization, due to their scaling potential and low power. A cryogenic digital signal processor backend with error correction logic would minimize the required output data rate at added power cost.

In the near term, it is desirable to have versatile cryogenic control and readout systems that can adapt to evolving qubit specifications. However, in the long-term the scope of cryogenic CMOS vs room temperature electronics should be defined, to enable large scale optimized control systems with low-latency error correction.